ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

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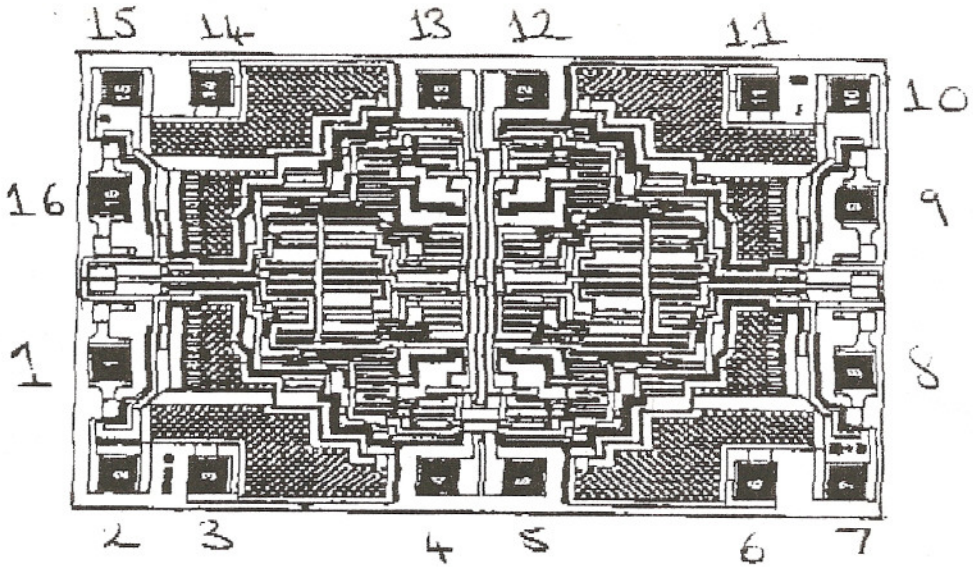
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Function	Pad	Function
1	IN_1	9	IN_3
2	D_1	10	D_3
3	S_1	11	S_3
4	V-	12	V_L
5	GND	13	V+
6	S_4	14	S_2
7	D_4	15	D_2
8	IN_4	16	IN_2

Topside Metal: Al
Backside: Si
Backside Potential: V+
Mask Ref: Issue 1
Bond Pads: .004" min.

APPROVED BY: CD	**DIE SIZE:.070" x .108"**	**DATE: 7/19/02**
MFG: Harris	**THICKNESS: .020"**	**P/N: DG413A**